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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Liu, et al.
Appl. No.	:	10/646,103
Filed	:	August 22, 2003
For	:	PASSIVATED MAGNETO-RESISTIVE BIT STRUCTURE AND PASSIVATION METHOD THEREFOR
Examiner	:	Marcos D. Pizarro Crespo
Group Art Unit	:	2814

REPLY BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is being submitted under 37 C.F.R. § 41.41 in response to the Examiner's Answer mailed on January 9, 2006. A Request for an Oral Hearing is being submitted with this Reply Brief.

Related Appeals and Interferences

Pursuant to 37 C.F.R. § 41.37(c)(2), Appellants hereby notify the Board of Patent Appeals that U.S. Patent Application No. 10/873,363 filed on June 21, 2004, which is now currently under appeal, may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Appellants, the Appellants Legal Representative, and the Assignee do not know of any other appeals or interferences that will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.

This Reply Brief is intended to supplement the arguments presented in Appellants' earlier brief. Because many of the issues raised in the Examiner's Answer have already been fully

briefed by Appellants, this Reply Brief only addresses certain new issues that are raised by the Examiner's Answer. Appellants and the Examiner continue to disagree over the teachings of U.S. Patent No. 5,861,328 by Tehrani, et al., ("Tehrani").

Two Distinct Processes

In the Examiner's Answer, the Examiner states that "Tehrani is using his figures to describe both processes." The Examiner later states that "figures 6 and 7 will be particular to the first process..." Appellants maintain the view that Tehrani's figures relate to the first process with the dielectric barrier and not to the second process with the conductive barrier.

Regardless, Appellants appreciate that the Examiner recognizes that Tehrani teaches two distinct processes. This is important, as will be discussed in further detail below.

The Differences Between the Processes are Material

The Examiner states that the "two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col. 5, ll. 34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col. 5/ll. 54-55)." The processes have significant differences as described below.

For example, the first process uses a dielectric layer for a barrier (Col. 5, lines 10-12) and optionally, a dielectric layer for an etch stop layer (Col. 5, lines 14-18).

Dielectric layers for barrier layers and/or etch stop layers are removed during the formation of vias 47 and 50 and prior to deposition of the metal system 55 (Col. 5, lines 34-50 and Col. 6, lines 13-15). With respect to dielectric layers, Tehrani teaches the "barrier layer is removed," during formation of vias 47 and 50 (Col. 5, line 48). Appellants note that a dielectric etch stop layer would be above the barrier layer (Col. 5, line 17) and would also be removed during formation of vias 47 and 50. By contrast, "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50." According to Tehrani, a conductive etch stop and passivation layer does not have to be removed during formation of vias 47 and 50.

For the dielectric layer process, Tehrani describes "vias 50 ***may extend*** outside or intersect the end of GMR element 41," (Col. 5, lines 37-38) (emphasis added). For the

conductive layer process, Tehrani describes that "via opening 50 must be enclosed by GMR memory element 41, that is the contact ***may not extend*** outside the ends of GMR memory element 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents," (Col. 5, lines 58-62) (emphasis added).

Accordingly, Appellants believe that the Examiner underestimates the distinctions between the two processes.

Via Openings 47

For the first time, the Examiner uses via openings 47 in rejecting the claims. Via openings 47 are for "metal interconnects 13," (Col. 5, lines 26-27) and have no bearing on whether a conductive etch stop barrier layer is on the side walls of a GMR bit.

Tehrani's Figures are Inconclusive

None of Tehrani's figures illustrate a conductive etch stop barrier layer, or even a dielectric etch stop layer or barrier layer. There is no figure that supports the Examiner's assertion of "[w]hat is clearly described in Tehrani is the fact that first layer of the cap layer 45 completely seals the bit 41 (see, *e.g.*, col. 5, ll. 4-8) and that in the second process, this first layer is CrSi, which is a conductive material (see, *e.g.*, col. 5, ll. 55-58 and col. 5, ll. 67- col. 6, ll. 2)."

While Tehrani's figures illustrate the dielectric system 45, there is no illustration of the location of an etch stop barrier layer. If the conductive etch stop layer were everywhere the dielectric cap 45 is shown as asserted by the Examiner, then the conductive etch stop layer would short circuit all the elements. This interpretation of a reference could not be reasonable.

Moreover, Appellants note again that the Examiner is combining attributes of the process for the dielectric barrier layer and the process for the conductive etch stop barrier layer. Appellants will discuss this in further detail later in this Reply.

The Location of Tehrani's Conductive Barrier Must be Inferred

Since Figure 5 and the other figures are not conclusive with respect to the conductive etch stop layer, then whether Tehrani teaches the presence or absence of the conductive etch stop layer on the side walls must be controlled by the teachings of the description.

Tehrani states, "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50," (Col. 6, lines 9-12). This illustrates that the etch stop and passivation layer is at least within the vias 50, i.e., on the top surface of the bits 41

Tehrani also states that "[v]ia opening 50 ***must be enclosed*** by GMR memory element 41, that is ***the contact may not extend outside the ends*** of GMR memory element 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents," (Col. 5, lines 58-62) (emphasis added). These "ends" correspond to Appellants' side walls. Appellants respectfully submit that if Tehrani's etch stop and passivation layer were present at the ends, then the etch stop and passivation layer would protect the ends and there would be no need for Tehrani's directive of "[v]ia opening 50 ***must be enclosed***" (Col. 5, line 58) (emphasis added). Accordingly, a logical inference can be made that the via opening 50 "must be enclosed" because the conductive etch stop and passivation layer does ***not*** encapsulate the ends or the side walls of the bit. Accordingly, Tehrani does not teach or suggest "each and every element" as required by 35 U.S.C. § 102(b).

The Examiner's "Embodiment" is an Unsupportable Combination

Appellants thus respectfully submit that the contrary characterization of Tehrani asserted by the Examiner is either factually incorrect, or it represents a legally-unsupported modification (or combination of embodiments) of Tehrani. Appellants further note that if the Examiner is modifying Tehrani, the appropriate statutory basis for a rejection of Claims 1, 8, or 12 could rest only on 35 U.S.C. § 103.

However, Appellants further note that "[e]ven when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2D 1313. Appellants respectfully submit that there has been no showing of a suggestion or motivation to modify the teachings of Tehrani, nor could the Examiner show such motivation, given Tehrani's teaching away from encapsulating the sidewalls with a conductive barrier by admonishing against exposing the "ends of GMR memory element 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents," (Col. 5, lines 60-62). Appellants respectfully

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submit that the Examiner is combining the attributes of the dielectric barrier layer process, in which Tehrani states "vias 50 ***may extend*** outside or intersect the end of GMR element 41," (Col. 5, lines 37-38) (emphasis added) with attributes of Tehrani's conductive etch stop barrier layer process, where Tehrani states "via opening 50 must be enclosed by GMR memory element 41, that is the contact ***may not extend*** outside the ends of GMR memory element 41," (Col. 5, lines 58-60) (emphasis added).

Accordingly, Appellants submit that Claims 1, 8, and 12 are patentably distinguished over the prior art and the Examiner's rejection of Claims 1, 8, and 12 should be reversed by the Board.

For the foregoing reasons, and the reasons set forth in Appellants' Appeal Brief, Appellants submit that the rejections are improper.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 9, 2006

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